

FIG. 1
(PRIOR ART)

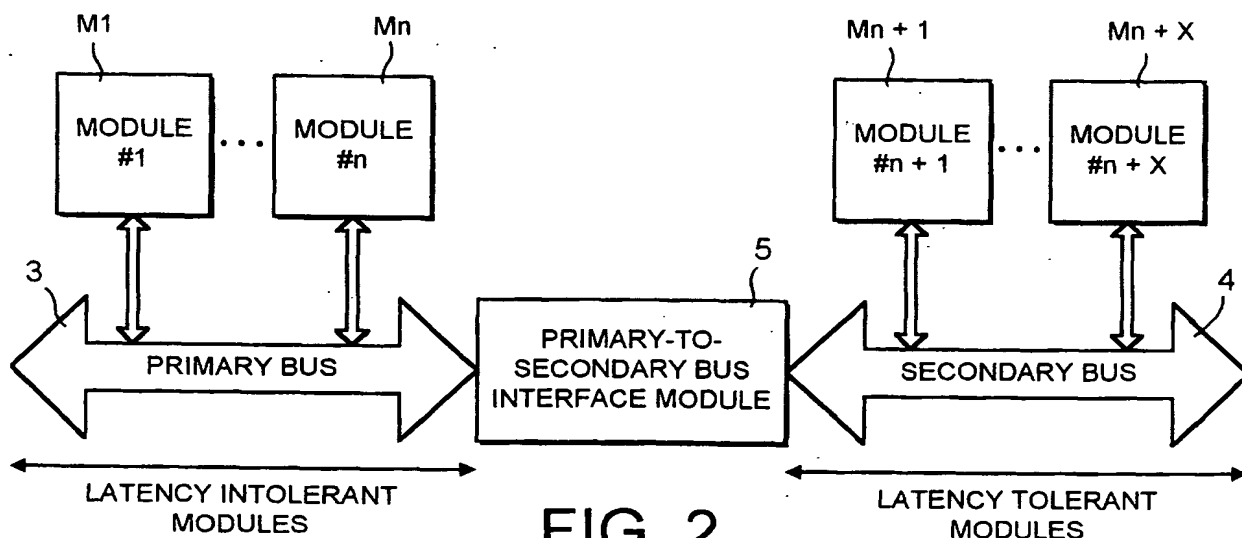


FIG. 2

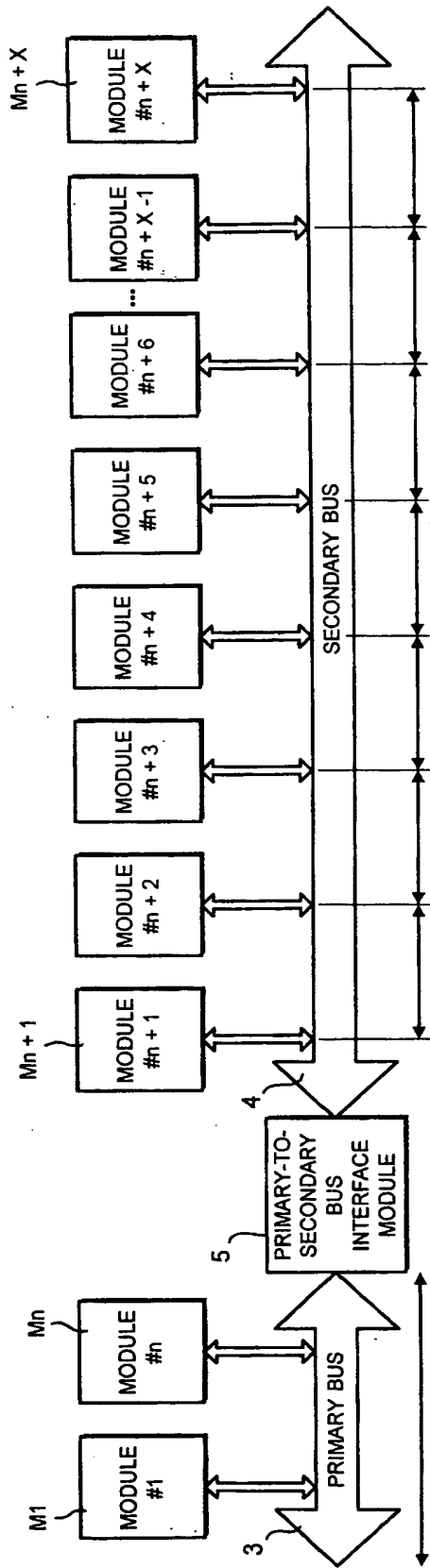


FIG. 3

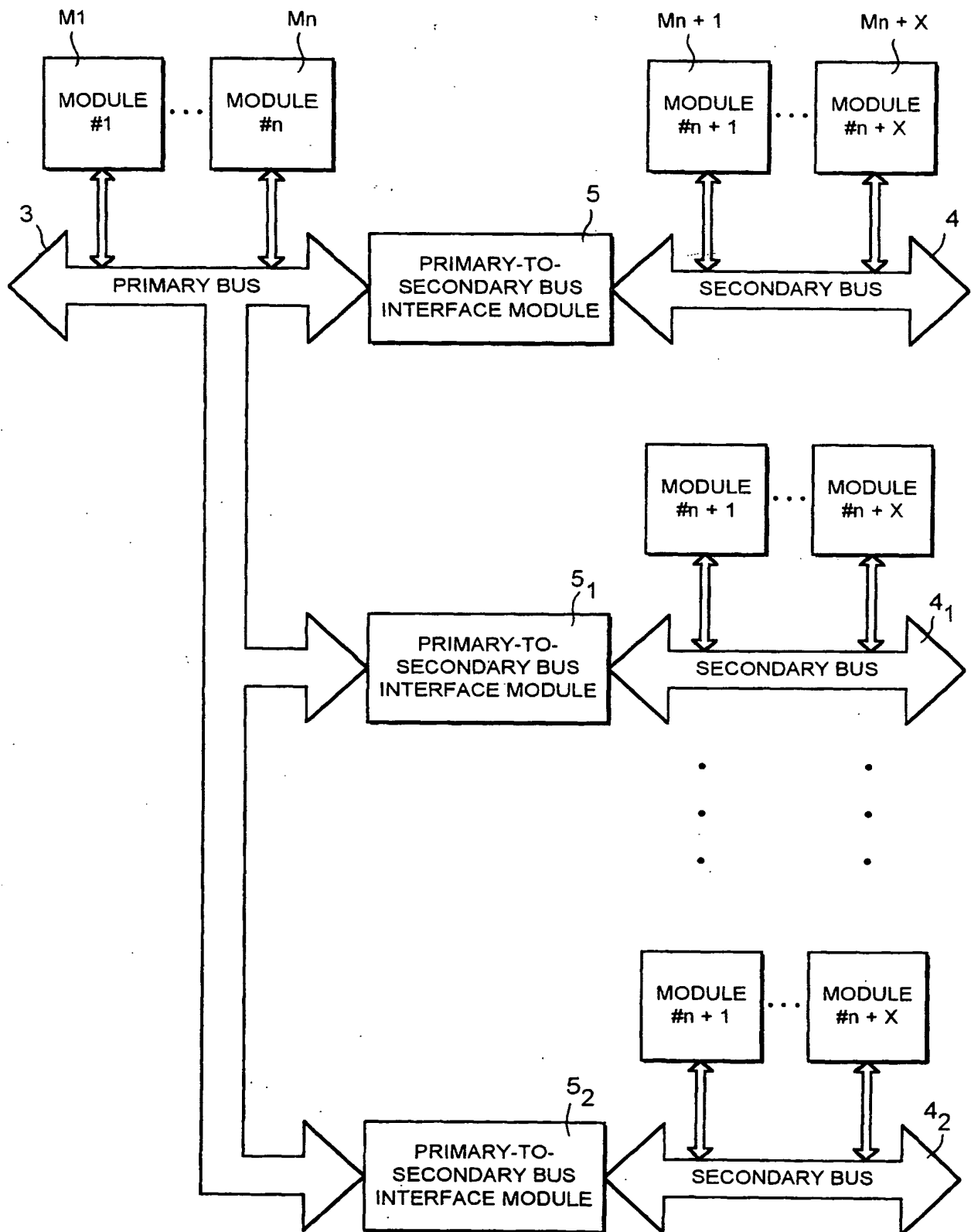


FIG. 4

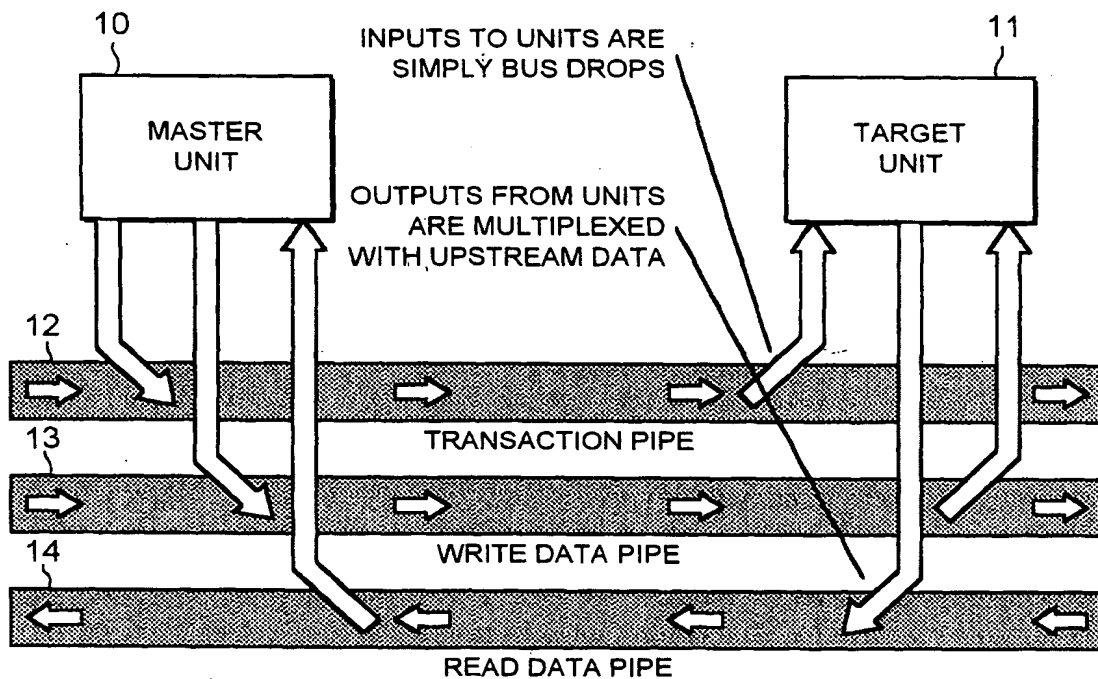


FIG. 5

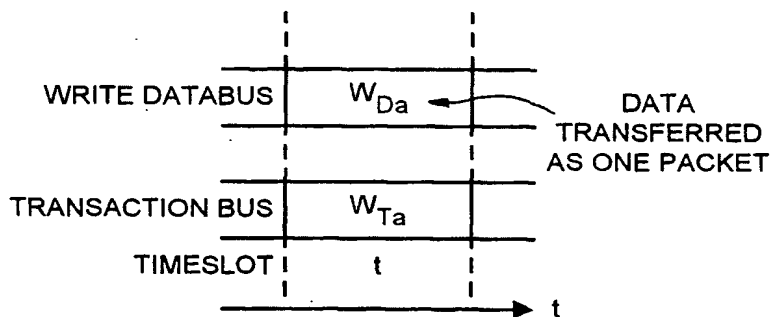


FIG. 6

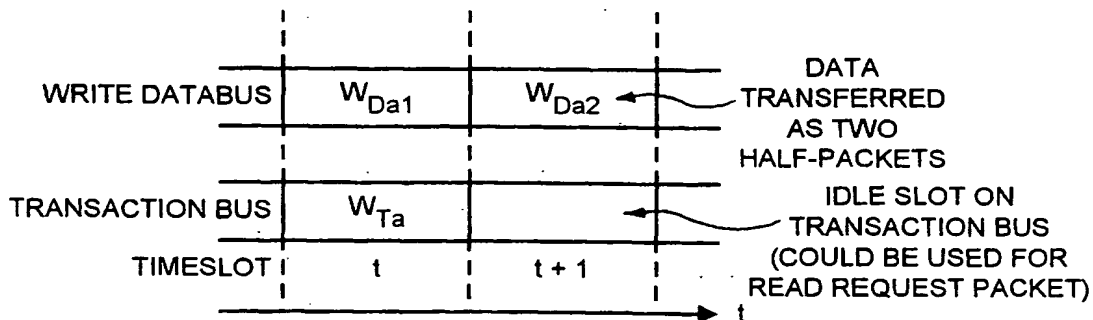


FIG. 7

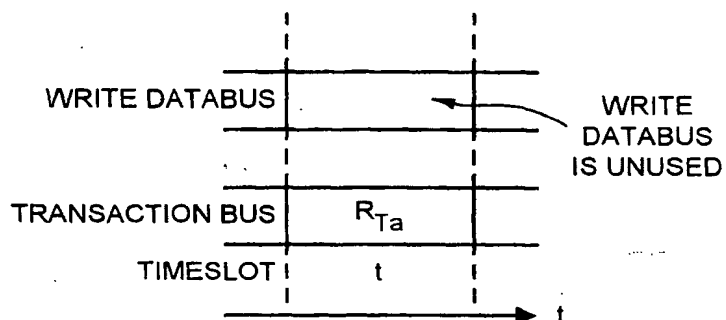


FIG. 8

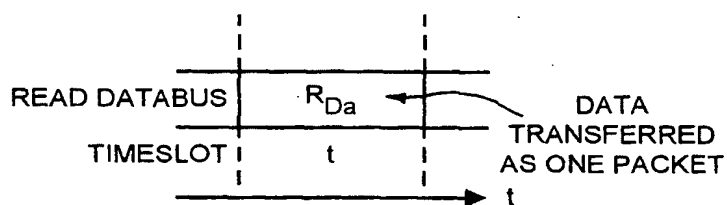


FIG. 9

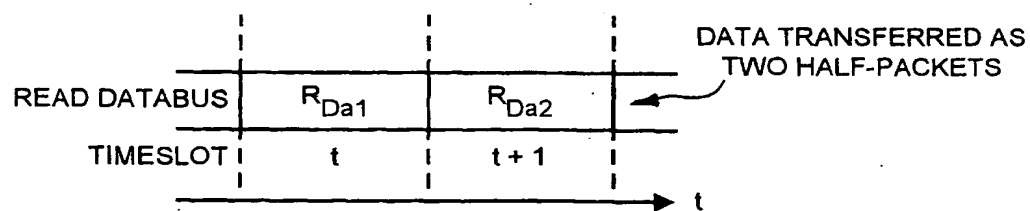
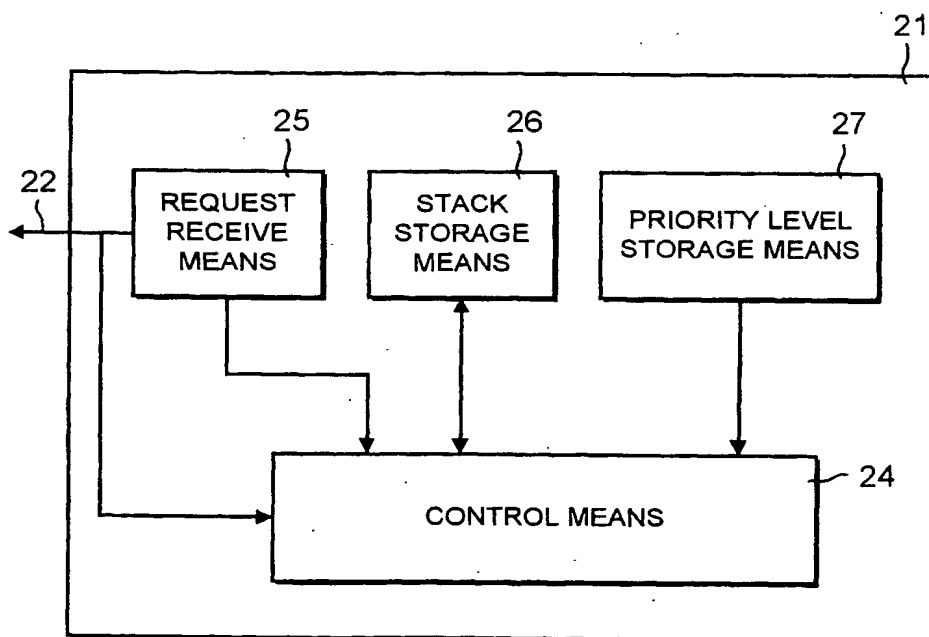
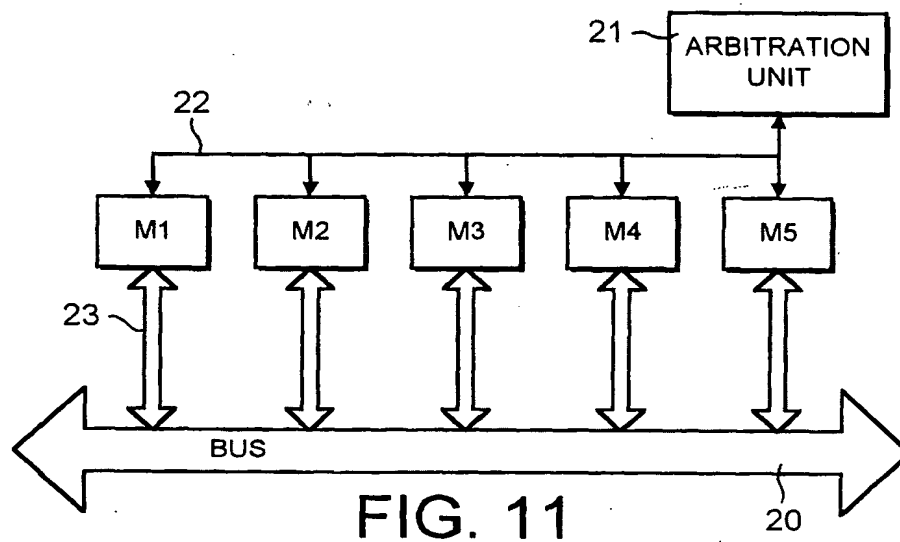


FIG. 10



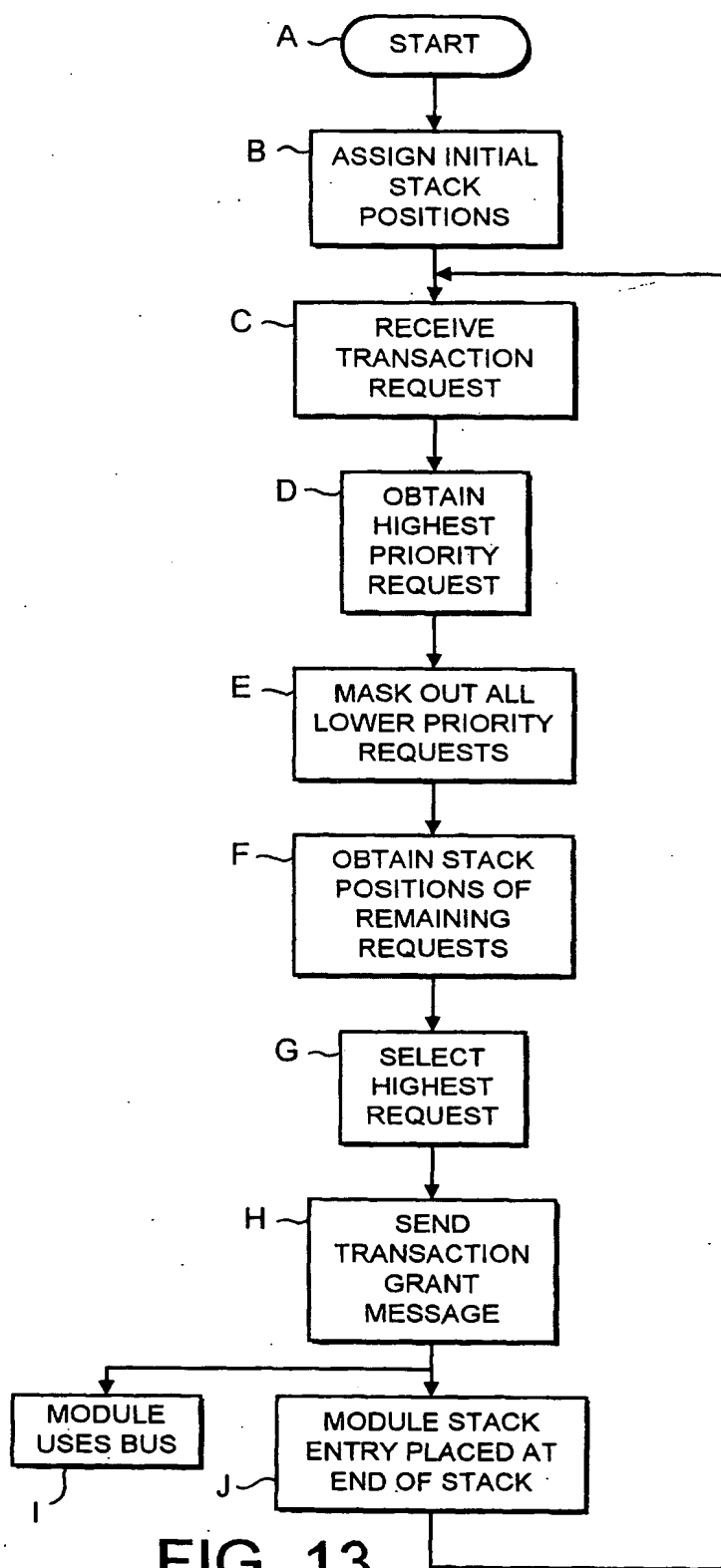


FIG. 13

28 MODULE	29 PRIORITY
M1	H
M2	M
M3	L
M4	H
M5	M

FIG. 14

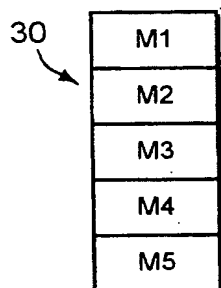


FIG. 15

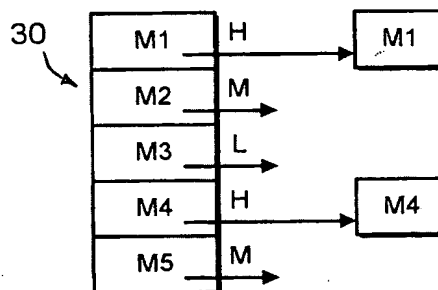


FIG. 16

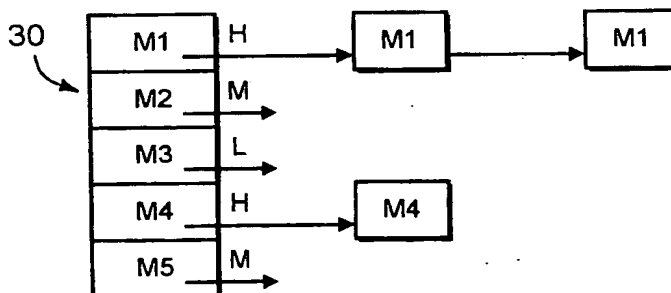


FIG. 17

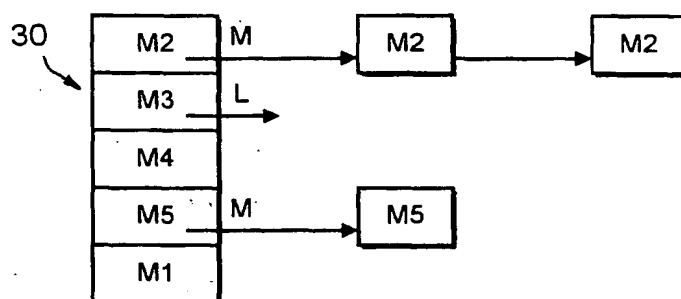


FIG. 18

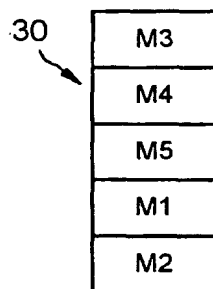


FIG. 19

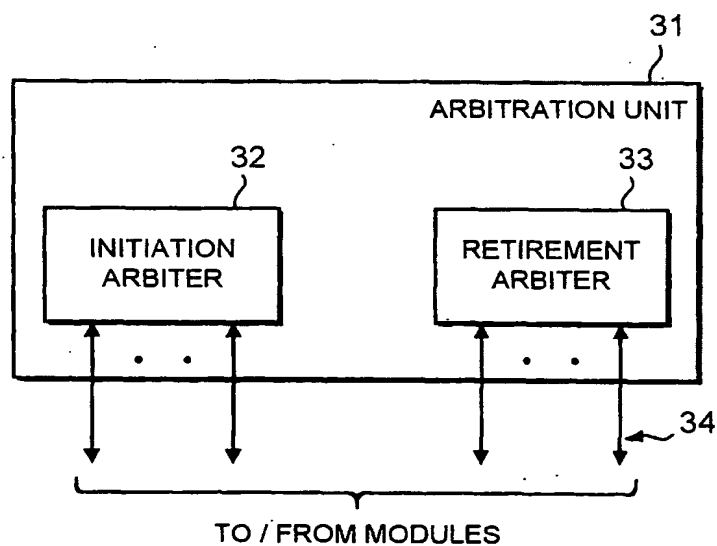


FIG. 20

35 ~ T	R1	W1	R2	W2	R3	W3
36 ~ W		W1A	W1B	W2A	W2B	W3A	W3B
37 ~ R				R1A	R1B		
TIME	t	t	t	t	t	t	t

FIG. 21

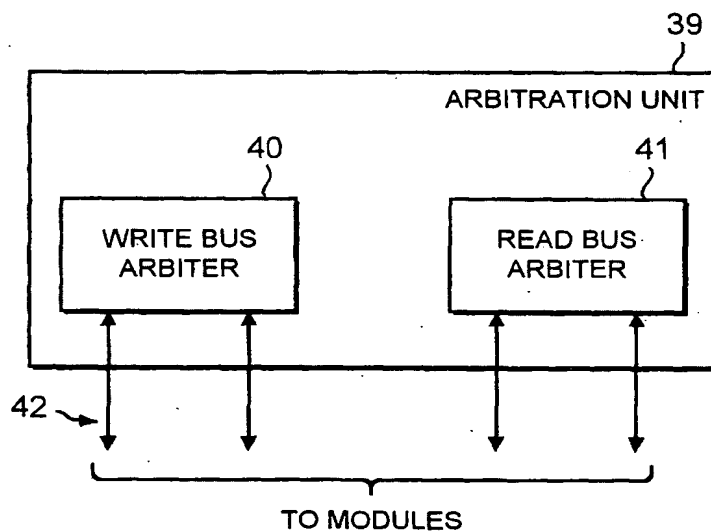


FIG. 22

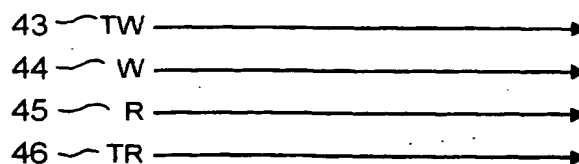


FIG. 23

43 ~ TW	W1		W2		W3	
44 ~ W	W1A	W1B	W2A	W2B	W3A	W3B
45 ~ R					R1A	R1B	R2A R2B
46 ~ TR	R1	R2	R3				
TIME →	t	t	t	t	t	t	

FIG. 24

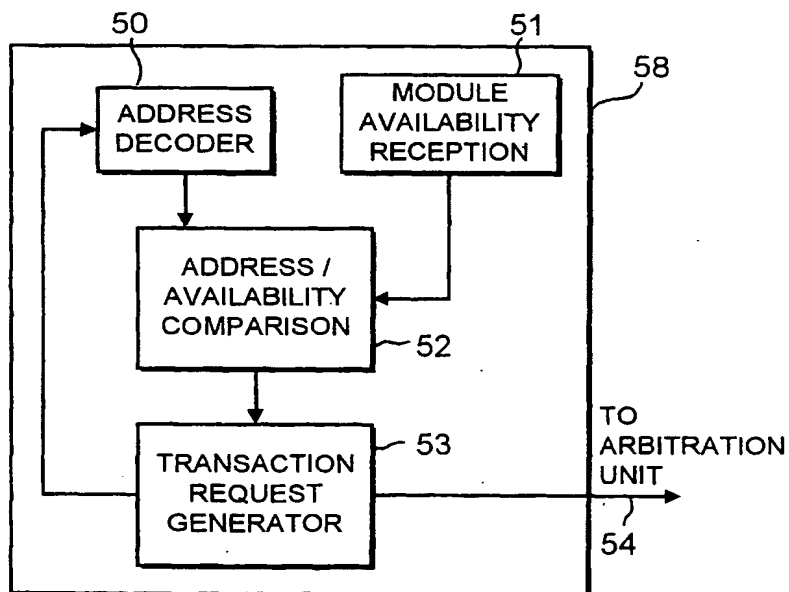


FIG. 25

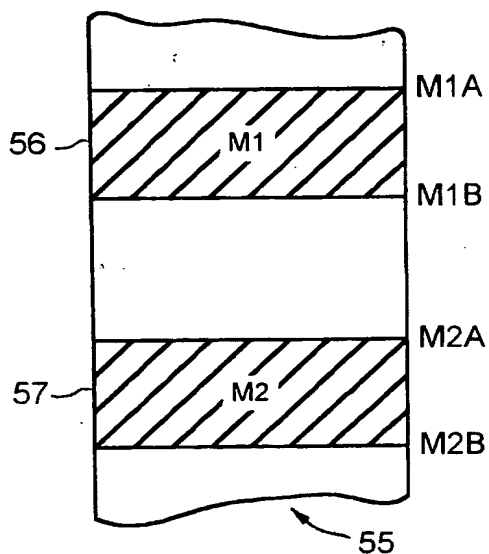


FIG. 26

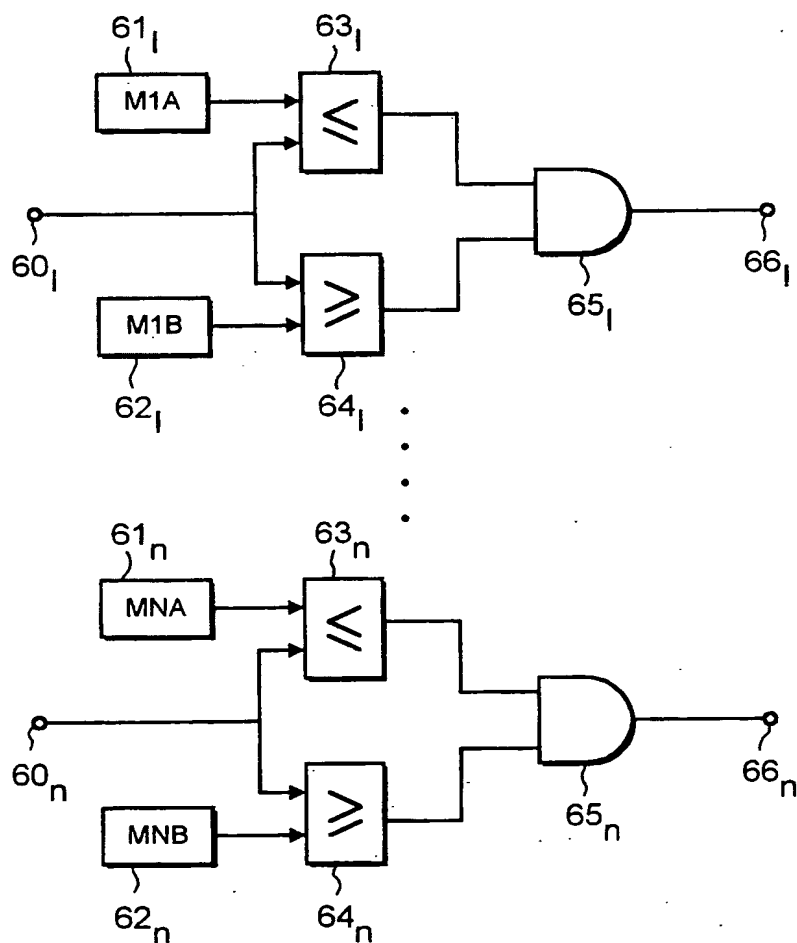


FIG. 27

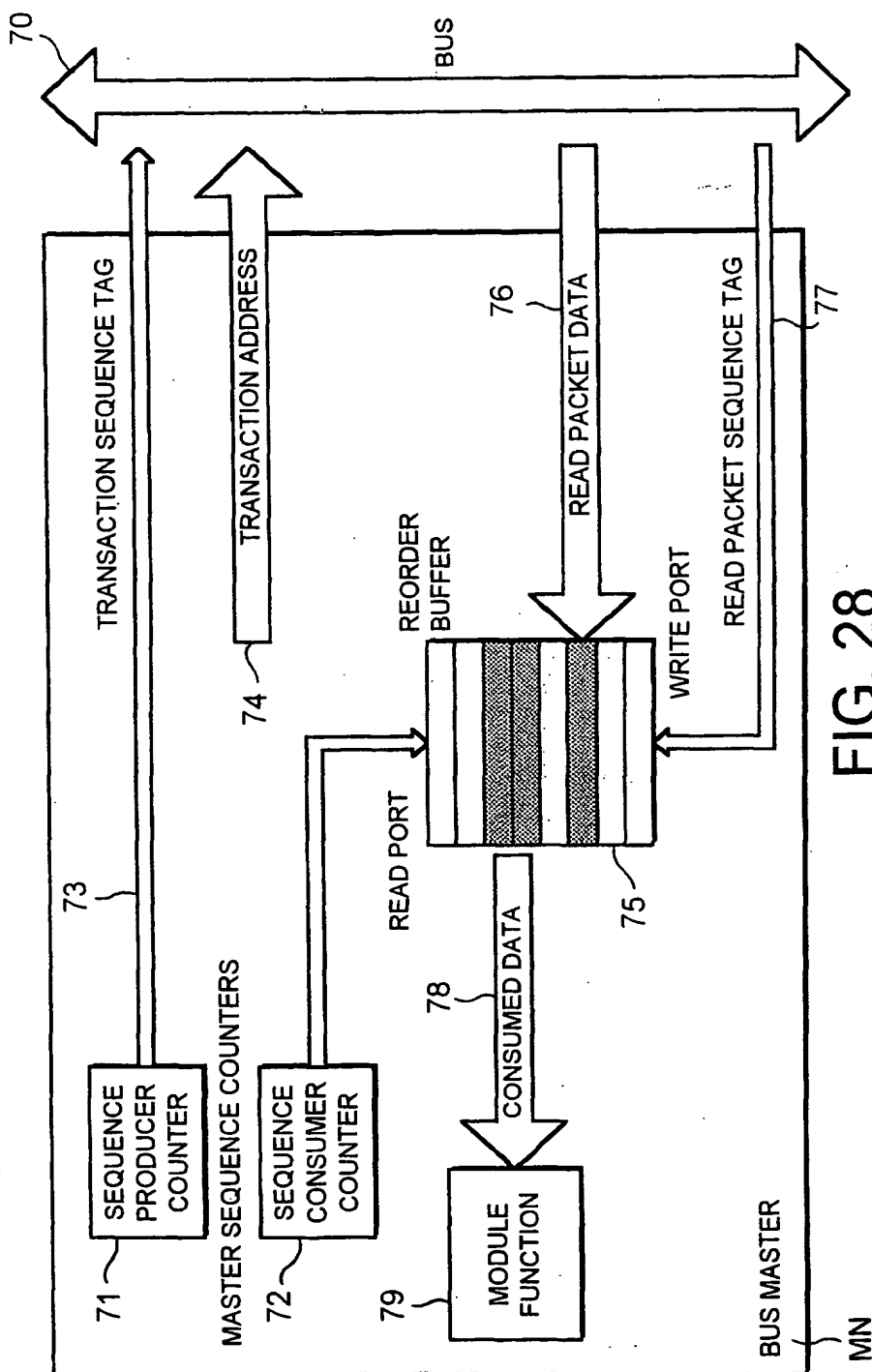


FIG. 28

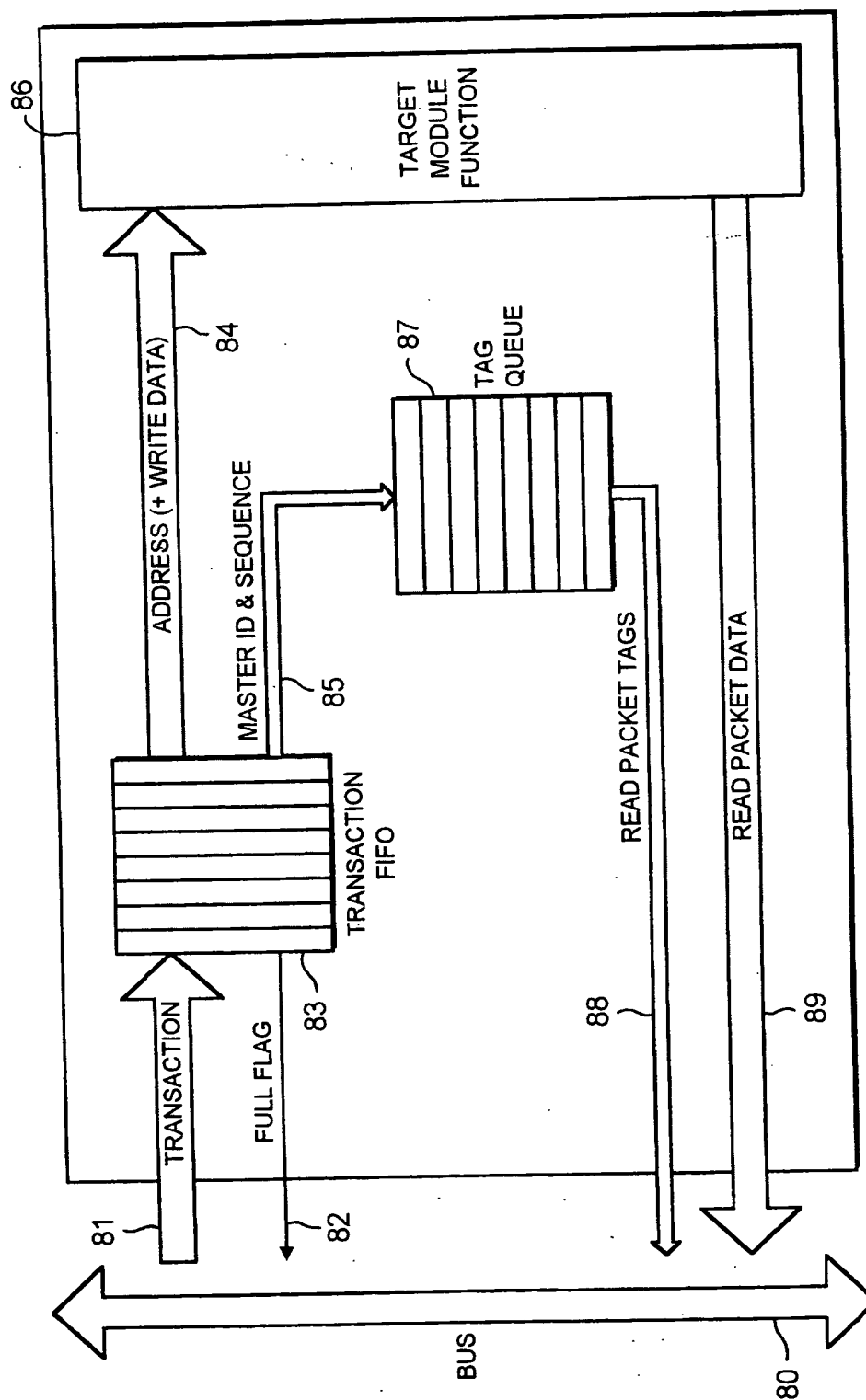


FIG. 29

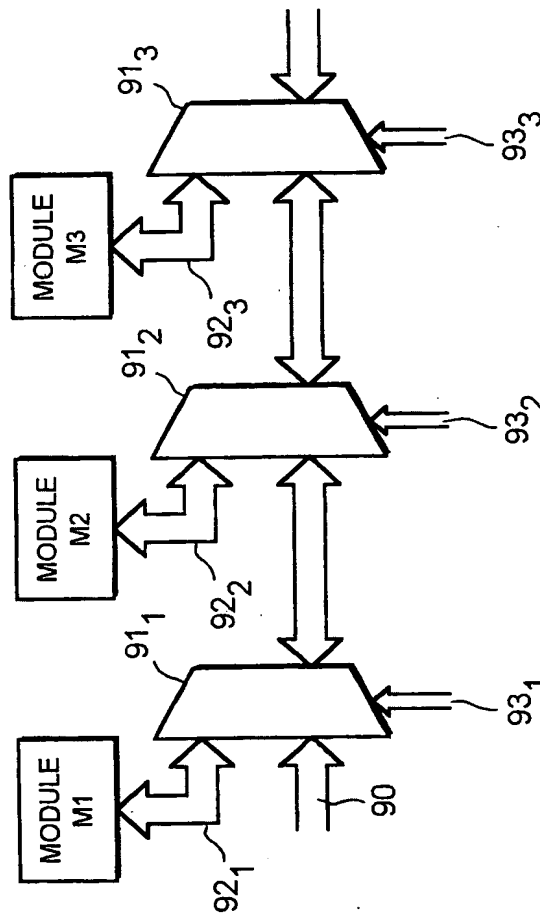


FIG. 30

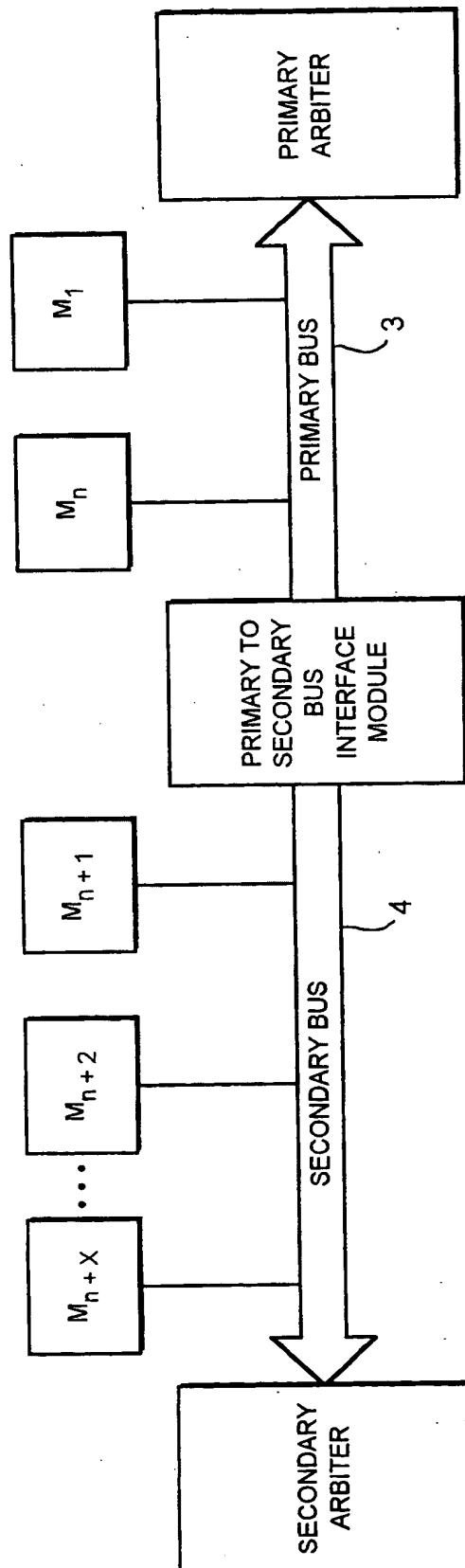


FIG. 31